Remarks

As stated above, the applicants appreciate the Examiner's thorough examination of the subject application and request reexamination and reconsideration of the subject application in view of the preceding amendments and the following remarks.

The Examiner asserts that the oath / declaration submitted in the subject application is defective, as the signature of inventor Delf Atallah is omitted. Applicants respectful disagree with this assertion and submit herewith a copy of the declaration previously submitted to the USPTO in the subject application. Specifically, this copy of the declaration was retrieved from the USPTO P.A.I.R website, includes the USPTO date stamp of 01 April 2002, and includes the signature of inventor Delf Atallah.

Concerning Item 4 of the subject action, the Examiner rejects claims 1-6, 9-12, 15-19, 22-26 and 29-33, under 35 USC §102(b), based on the teachings of Anderson (U.S. Patent No. 5,898,869; hereinafter Anderson).

Applicants claim (in currently amended claim 1):

> 1. (Currently Amended) A system comprising: a core processing circuit; and a host processing system coupled to the core processing circuit through a host bridge, the host processing system comprising: logic to maintain the core processing circuit in a reset state during power up of the core processing circuit; and logic to load a reset vector to one or more registers at a boot address associated with the core processing circuit, the reset vector comprising one or more instructions to fetch additional instructions to initialize the core processing circuit upon release from the reset state; ***wherein the host processing system further comprises a system memory and logic to set an address translation unit to fetch instructions from the system memory in response to requests from the core processing circuit.*** *Emphasis Added*

Applicants claim (in currently amended claim 9):

> 9. (Currently Amended) A method comprising: having a host processing system maintain a core processing circuit in a reset state during power up of the core processing circuit; loading a reset vector to one or more registers at a boot address associated with the core processing circuit, the reset vector comprising one or more instructions to fetch additional instructions from a system memory coupled to the core processing circuit through a host bridge of a host processing system; and ***setting an address translation unit to fetch instructions from the***

system memory in response to requests from the core processing circuit. *Emphasis Added*

Applicants claim (in currently amended claim 15):

15. (Currently Amended) A method comprising: having a host processing system maintain a core processing circuit in a reset state during power up of the core processing circuit; loading instructions from a system memory of a host processing system to one or more registers at a boot address associated with the core processing circuit, the instructions comprising one or more instructions to initialize the core processing circuit upon release of the core processing circuit from the reset state; and ***setting an address translation unit to fetch instructions from the system memory in response to requests from the core processing circuit.*** *Emphasis Added*

Applicants claim (in currently amended claim 22):

22. (Currently Amended) An article comprising: a storage medium comprising machine-readable instructions encoded there on for: having a host processing system maintain a core processing circuit in a reset state during power up of the core processing circuit; loading a reset vector to one or more registers at a boot address associated with the core processing circuit, the reset vector comprising one or more instructions to fetch additional instructions from a system memory coupled to the core processing circuit through a host bridge of a host processing system; and ***setting an address translation unit to fetch instructions from the system memory in response to requests from the core processing circuit.*** *Emphasis Added*

Applicants claim (in currently amended 29):

29. (Currently Amended) An article comprising: a storage medium comprising machine-readable instructions encoded there on for: having a host processing system maintain a core processing circuit in a reset state during power up of the core processing circuit; and loading instructions from a system memory of a host processing system to one or more registers at a boot address associated with the core processing circuit, the instructions comprising one or more instructions to initialize the core processing circuit upon release from the reset state; and ***setting an address translation unit to fetch instructions from the system memory in response to requests from the core processing circuit.*** *Emphasis Added*

Applicants respectfully assert that Anderson fails to disclose the emphasized element of applicants' claim 1, "*wherein the host processing system further comprises a system memory and logic to set an address translation unit to fetch instructions from the system memory in response*

to requests from the core processing circuit". Further, applicants respectfully assert that Anderson fails to disclose the emphasized element of applicants' claim 9, namely "*setting an address translation unit to fetch instructions from the system memory in response to requests from the core processing circuit*". Additionally, applicants respectfully assert that Anderson fails to disclose the emphasized element of applicants' claim 15, namely "*setting an address translation unit to fetch instructions from the system memory in response to requests from the core processing circuit*". Further, applicants respectfully assert that Anderson fails to disclose the emphasized element of applicants' claim 22, namely "*setting an address translation unit to fetch instructions from the system memory in response to requests from the core processing circuit*". Finally, applicants respectfully assert that Anderson fails to disclose the emphasized element of applicants' claim 29, namely "*setting an address translation unit to fetch instructions from the system memory in response to requests from the core processing circuit*".

Accordingly, applicants respectfully assert that Anderson is not a proper basis for a 35 USC §102(b) rejection, as the reference fails to disclose each and every element of the applicants' claimed invention.

Applicants have cancelled dependent claims 4, 11, 19, 24 and 33 and moved the subject matter of these cancelled claims into independent claim 1, 9, 15, 22, and 29 respectively. The Examiner had rejected (now cancelled) dependent claims 4, 11, 19, 24 and 33 based upon the teaching of Anderson. Specifically, the Examiner relied on Anderson, Column 2, Lines 48-50 that discloses:

> The boot logic may then include address decode circuitry ***responsive to a particular address presented by the host*** for releasing the processor execution and causing the processor to boot. *See Anderson, Column 2, Lines 48-50; Emphasis Added*

Additionally, concerning the address decode circuitry, Anderson discloses:

> In one embodiment, dual-ported memory 39 may also be used for semaphore based communications between host 11 and processor 31. Accordingly, dual-ported memory 39 includes multiple (for example, sixteen) semaphore registers with associated logic. Addressing of the semaphore registers is provided by selecting a semaphore or memory address space within the dual-ported memory using a control input thereof. Conventional address decode circuitry provides this selection through memory mapping in accordance with the present invention.

Accordingly, Anderson discloses address decode circuitry that is "***responsive to a particular address presented by the host***". Conversely, applicants claim "setting an address translation unit to fetch instructions from the system memory ***in response to requests from the core processing circuit***". Applicants respectfully assert that Anderson fails to disclose such a system.

Accordingly, applicants respectfully assert that Anderson is not a proper basis for a 35 USC §102(b) rejection, as the reference fails to disclose each and every element of applicants' currently-amended claims 1, 9, 15, 22 and 29. Therefore, the applicants respectfully assert that independent claims 1, 9, 15, 22 and 29 are patentable over the cited reference.

Further, as dependent claims 2-3 and 5-8 depend (either directly or indirectly) upon independent claim 1, applicants respectfully assert that claims 2-3 and 5-8 are also patentable over the cited reference. Additionally, as dependent claims 10 and 12-14 depend (either directly or indirectly) upon independent claim 9, applicants respectfully assert that claims 10 and 12-14 are also patentable over the cited reference. Further, as dependent claims 16-18 and 20-21 depend (either directly or indirectly) upon independent claim 15, applicants respectfully assert that claims 16-18 and 20-21 are also patentable over the cited reference. Additionally, as dependent claims 23 and 25-28 depend (either directly or indirectly) upon independent claim 22, applicants respectfully assert that claims 23 and 25-28 are also patentable over the cited reference. Finally, as dependent claims 30-32 and 34-35 depend (either directly or indirectly) upon independent claim 29, applicants respectfully assert that claims 30-32 and 34-35 are also patentable over the cited reference.

Concerning Item 5 of the subject action, the Examiner rejects claims 7, 13, 20, 27 and 34, under 35 USC §103(a), based on the teachings of Anderson.

For the reasons discussed above, the applicants respectfully assert that Anderson fails to disclose the emphasized element of applicants' claim 1, "*wherein the host processing system further comprises a system memory and logic to set an address translation unit to fetch instructions from the system memory in response to requests from the core processing circuit*". Further, applicants respectfully assert that Anderson fails to disclose the emphasized element of applicants' claim 9, namely "*setting an address translation unit to fetch instructions from the system memory in response to requests from the core processing circuit*". Additionally,

applicants respectfully assert that Anderson fails to disclose the emphasized element of applicants' claim 15, namely "*setting an address translation unit to fetch instructions from the system memory in response to requests from the core processing circuit*". Further, applicants respectfully assert that Anderson fails to disclose the emphasized element of applicants' claim 22, namely "*setting an address translation unit to fetch instructions from the system memory in response to requests from the core processing circuit*". Finally, applicants respectfully assert that Anderson fails to disclose the emphasized element of applicants' claim 29, namely "*setting an address translation unit to fetch instructions from the system memory in response to requests from the core processing circuit*".

As dependent claim 7 depends (either directly or indirectly) upon independent claim 1, dependent claim 13 depends (either directly or indirectly) upon independent 9, dependent claim 20 depends (either directly or indirectly) upon independent claim 15, dependent claim 27 depends (either directly or indirectly) upon independent 22, and dependent claim 34 depends (either directly or indirectly) upon independent 29, the applicants respectfully assert that claims 7, 13, 20, 27 and 34 are also patentable over the cited reference.

Concerning Item 6 of the subject action, the Examiner further rejects claims 8, 14, 21, 28 and 35, under 35 USC §103(a), based on the combination of the teachings of Anderson, and Klein (U.S. Patent No. 6,226,224; hereinafter Klein).

For the reasons discussed above, the applicants respectfully assert that Anderson fails to disclose the emphasized element of applicants' claim 1, "*wherein the host processing system further comprises a system memory and logic to set an address translation unit to fetch instructions from the system memory in response to requests from the core processing circuit*". Further, applicants respectfully assert that Anderson fails to disclose the emphasized element of applicants' claim 9, namely "*setting an address translation unit to fetch instructions from the system memory in response to requests from the core processing circuit*". Additionally, applicants respectfully assert that Anderson fails to disclose the emphasized element of applicants' claim 15, namely "*setting an address translation unit to fetch instructions from the system memory in response to requests from the core processing circuit*". Further, applicants respectfully assert that Anderson fails to disclose the emphasized element of applicants' claim 22, namely "*setting an address translation unit to fetch instructions from the system memory in*

response to requests from the core processing circuit". Finally, applicants respectfully assert that Anderson fails to disclose the emphasized element of applicants' claim 29, namely "*setting an address translation unit to fetch instructions from the system memory in response to requests from the core processing circuit*".

As dependent claim 8 depends (either directly or indirectly) upon independent claim 1, dependent claim 14 depends (either directly or indirectly) upon independent 9, dependent claim 21 depends (either directly or indirectly) upon independent claim 15, dependent claim 28 depends (either directly or indirectly) upon independent 22, and dependent claim 35 depends (either directly or indirectly) upon independent 29, the applicants respectfully assert that claims 8, 14, 21, 28 and 35 are also patentable over the cited reference.

No new matter has been added by these amendments. While the applicants respectfully assert that the subject application is now in condition for allowance, the Examiner is invited to telephone applicants' attorney (603-668-6560) to facilitate prosecution of this application. Please apply any charges or credits to deposit account 50-2121.

Respectfully submitted,

MARK A. SCHMISSEUR

By his Representatives,

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Date 1/20/06

By _____
Edmund P. Pfleger
Reg. No. 41,252

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 20 day of January 2005.

Kyrstin Ryan
Name

Kyrstin Ryan
Signature

Enclosure: Copy of Declaration signed by all inventors

(3)

Attorney's Docket No.: 42390P12808

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION (FOR INTEL CORPORATION PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SYSTEM AND METHOD OF REMOTELY INITIALIZING A LOCAL PROCESSOR

the specification of which

☐ is attached hereto.

☒ was filed on December 26, 2001 as
United States Application Number 10/032,762
or PCT International Application Number _____
and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application. I do not know and do not believe that the claimed invention was in public use or on sale in the United States of America more than one year prior to this application, nor do I know or believe that the invention has been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

APPLICATION NUMBER	COUNTRY (OR INDICATE IF PCT)	DATE OF FILING (day, month, year)	PRIORITY CLAIMED
			☐ No ☐ Yes
			☐ No ☐ Yes
			☐ No ☐ Yes

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

APPLICATION NUMBER	FILING DATE

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION NUMBER	FILING DATE	STATUS (ISSUED, PENDING, ABANDONED)

I hereby appoint BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP, a firm including: Ramin Aghevli, Reg. No. 43,462; William E. Alford, Reg. No. 37,764; Farzad E. Amini, Reg. No. 42,261; William Thomas Babbitt, Reg. No. 39,591; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; R. Alan Burnett, Reg. No. 46,149; Gregory D. Caldwell, Reg. No. 39,926; Thomas M. Coester, Reg. No. 39,637; Robert P. Cogan, Reg. No. 25,049; Donna Jo Coningsby, Reg. No. 41,684; Florin A. Corie, Reg. No. 46,244; James K. Dawson, Reg. No. 41,701; Dennis M. deGuzman, Reg. No. 41,702; Stephen M. De Klerk, Reg. No. P46,503; Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Justin M. Dillon, Reg. No. 42,486; Sanjeet Dutta, Reg. No. 46,145; Matthew C. Fagan, Reg. No. 37,542; Tarek N. Fahmi, Reg. No. 41,402; Mark C. Farrell, Reg. No. 45,988; George Fountain, Reg. No. 36,374; James Y. Go, Reg. No. 40,621; James A. Henry, Reg. No. 41,064; Willmore F. Holbrow III, Reg. No. 41,845; Sheryl Sue Holloway, Reg. No. 37,850; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; William W. Kidd, Reg. No. 31,772; Walter T. Kim, Reg. No. 42,731; Eric T. King, Reg. No. 44,188; Steven Laut, Reg. No. 47,736; Samuel S. Lee, Reg. No. 42,791; Gordon R. Lindeen III, Reg. No. 33,192; Jan Carol Little, Reg. No. 41,181; Julio Loza, Reg. No. 47,758; Joseph Lutz, Reg. No. 43,765; Lawrence Lycke, Reg. No. 38,540; Michael J. Mallie, Reg. No. 36,591; Andre L. Marais, under 37 C.F.R. § 10.9(b); Raul D. Martinez, Reg. No. 46,904; Paul A. Mendonsa, Reg. No. 42,879; Clive D. Menezes, Reg. No. 45,493; Richard A, Nakashima, Reg. No. 42,023; Chun M. Ng, Reg. No. 36,878; Thien T. Nguyen, Reg. No. 43,835; Thinh V. Nguyen, Reg. No. 42,034; Robert B. O'Rourke, Reg. No. P46,972; Daniel E. Ovanezian, Reg. No. 41,236; Gregg A. Peacock, Reg. No. 45,001; Marina Portnova, Reg. No. P45,750; Michael A. Proksch, Reg. No. 43,021; Randol W. Read, Reg. No. 43,876; William F. Ryann, Reg. 44,313; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Jeffrey S. Schubert, Reg. No. 43,098; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Judith A. Szepesi, Reg. No. 39,393; Ronald S. Tamura, Reg. No. 43,179; Edwin H. Taylor, Reg. No. 25,129; Lance A. Termes, Reg. No. 43,184; John F. Travis, Reg. No. 43,203; Kerry D. Tweet, Reg. No. 45,959; Mark C. Van Ness, Reg. No. 39,865; Thomas A. Van Zandt, Reg. No. 43,219; Lester J. Vincent, Reg. No. 31,460; Glenn E. Von Tersch, Reg. No. 41,364; John Patrick Ward, Reg. No. 40,216; Mark L. Watson, Reg. No. P46,322; Thomas C. Webster, Reg. No. P46,154; and Norman Zafman, Reg. No. 26,250; my patent attorneys, and Firasat Ali, Reg. No. 45,715; Jonathan Miller, Reg. No. 48,534; and Brent Vecchia, Reg. No. 48,011; my patent agents, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, and Alan K. Aldous, Reg. No. 31,905; Ed Brake, Reg. No. 37,784; Ben Burge, Reg. No. 42,372; Robert A. Burtzlaff, Reg. No. 35,466; Richard C. Calderwood, Reg. No. 35,468; Jeffrey S. Draeger, Reg. No. 41,000; Cynthia Thomas Faatz, Reg No. 39,973; Jeffrey B. Huter, Reg. No. 41,086; John Kacvinsky, Reg. No. 40,040; Seth Z. Kalson, Reg. No. 40,670; David J. Kaplan, Reg. No. 41,105; Peter Lam, Reg. No. 44,855; Anthony M. Martinez, Reg. No. 44,223; Charles A. Mirho, Reg. No. 41,199; Paul Nagy, Reg. No. 37,896; Leo V. Novakoski, Reg. No. 37,198; Thomas C. Reynolds, Reg. No. 32,488; Kenneth M. Seddon, Reg. No. 43,105; Mark Seeley, Reg. No. 32,299; Steven P. Skabrat, Reg. No. 36,279; Howard A. Skaist, Reg. No. 36,008; Robert G. Winkle, Reg. No. 37,474; Sharon Wong, Reg. No. 37,760; Steven D. Yates, Reg. No. 42,242; Calvin E. Wells; Reg. No. 43,256 and Charles K. Young, Reg. No. 39,435; my patent attorneys, and my patent agents, of INTEL CORPORATION, with offices located at 2200 Mission College Blvd., Santa Clara, CA 95052, telephone (408)765-8080; with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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